Grid Dip Oscillator - Project Notes

Update July 2013

This project was based on an original design by Harry Lythell SM0VPO (a one-time member of CDARC) who is gratefully acknowledged here. Some references and comments below may be out of date.
Harry's design may now be found at:
http://www.sm0vpo.com - Projects - GDO and Uses

M0BLP SM0VPO's GDO 17/04/01

M0BLP's Implementation of the SM0VPO

Notes on the Design/Layout

1. The PCB mounts directly on the back of VC1.
2. VC1 can be glued to the side of the case provided.
3. Be careful when laying out the components inside the case. Keep all leads short for the best results.
4. SM0VPO talks about a BC245 FET, but this should be a BF245.
5. The circuit diagram and description by SM0VPO have some inconsistencies e.g. the variable capacitor referred to as either C1a,b,c,d or C2a,b,c,d. On my layout VC1 corresponds to C1a,b,c,d where C1a=C1, C1b=C2, C1c=FC1 and C1d=FC2. Note that the two ground tags are different sizes to prevent incorrect insertion into the PCB. Be sure to drill your PCB correctly. The labels C1,C2,FC1 and FC2 are written into the back plastic cover of VC1.
6. The potentiometer (VR1) includes a switch which can be used in the battery positive lead.
7. A useful addition to the circuit may be a DPST switch for shorting DIN socket pins 3-5 and 1-4.
8. VR1 is now 50k.
9. The meter is 250uA f.s.d.
10. VC1 is now C1,2=160pF and FC1,2=50pF max. This was the closest value easily obtainable (Rapid Electronics part 12-0250).
11. Coil winding may need some experimentation!

Connector Pinouts

- J1 - PP3 Battery Clip

1	*2*
Positive	Negative

- J2 - Meter/Potentiometer Connector

J2 *1*	*2*	*3*
Positive end of the Pot.	One side of the meter	Negative side of the Pot.

- J3 - 270degree DIN Socket

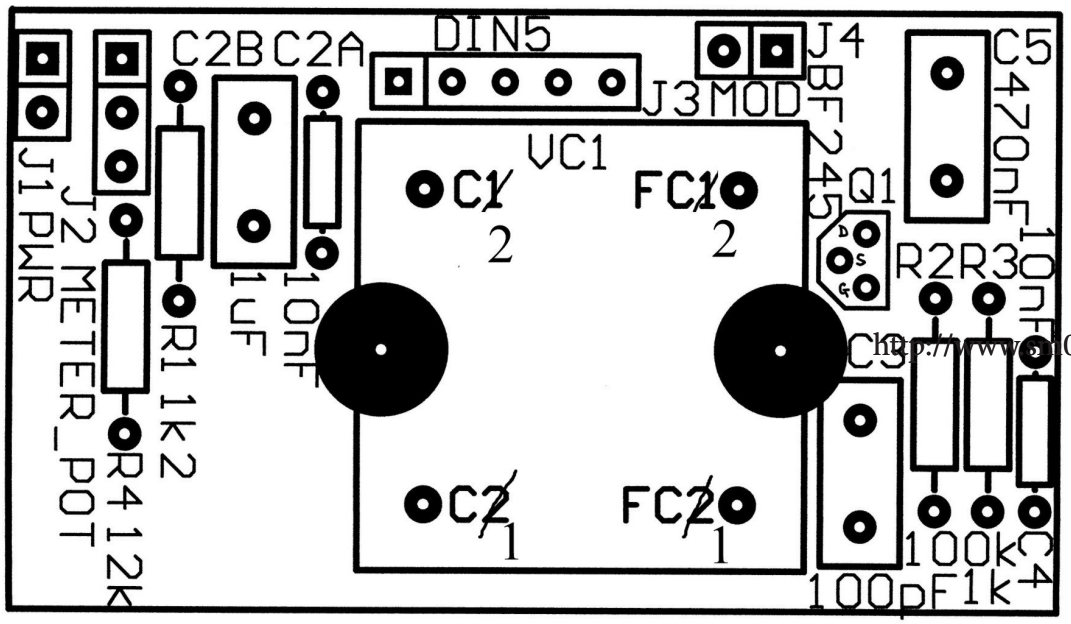
1	*2*	*3*	*4*	*5*
DIN pin1 (VC1[C2])	DIN pin 2 (C2a,b)	DIN pin3 (VC1[C1])	DIN pin4 (VC1[FC2])	DIN pin5 (VC1[FC1])

- J4 - Modulation Input

1	*2*
Mod. Input	Ground

Website

The circuit diagram can be found at:
http://hem.passagen.se/sm0vpo/use/gdo.htm



PCB LAYOUT FOR THE SM0VPO GDO.

M0BLP

17/4/2001

PLEASE NOTE

Issues with the GDO:

1. Note that M0BLP entered the PCB footprint for the variable capacitor whilst looking at the pin view of this device. However symmetry came to our rescue, so on the PCB overlay just reverse the VC1 labelling for pins C1/C2 and FC1/FC2.

2. M0BLP found that a 100pF capacitor from the Drain of the JFET could be used to couple the GDO to the PIC-FC1 frequency counter A input.